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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,872	04/20/2004	Kenneth C. Creta	42P18867	5618

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EXAMINER	
UNELUS, ERNEST	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 07/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/828,872	CRETA ET AL.	
	Examiner	Art Unit	
	Ernest Unelus	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
7/23/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10/828,872 has a total of 36 claims pending in the application; there are 5 independent claims and 31 dependent claims, all of which are ready for examination by the examiner.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. INFORMATION CONCERNING DRAWINGS

Drawings

3. The applicant's drawings submitted are acceptable for examination purposes.

III. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 1-36** are rejected under 35 U.S.C. 102(e) as being anticipated by Grun (US pat. 6,629,166).

6. As per **claim 1**, Grun discloses "A method comprising: receiving a plurality of write transactions from a processor **(see fig. 2, which discloses write transaction from the processor (initiator) 20 to the target channel adapter 22, see also col. 7, lines 1-13)**; storing data associated with the write transactions to a buffer of an input/output (I/O) hub **(see fig. 3, which discloses buffering incoming data inside the I/O hub 22 from the initiator)**; and flushing the data to an I/O device according to a protocol between the I/O hub and the processor **(see fig. 3, which discloses transmitting data from the I/O hub 22 to an I/O controller within the target)**.

7. As per **claims 2, 13, 22, and 35**, Grun discloses "The method of claim 1," **[See rejection to claim 1 above]**, wherein flushing the data to the I/O device includes: determining whether a flush signal has been received from the processor **(col. 7, lines 52-55, discloses "The I/O controller 24, in turn, uses the services of the channel-based switched fabric to fulfill that request and to notify the initiator 20 that the request has been completed")**; and flushing the data if the flush signal has been received **(col. 7, lines 50-55, transmitting a receive signal (the flush signal) from the initiator)**, the protocol including an signaling protocol **(fig. 5 discloses a signaling protocol from the initiator)**.

8. As per **claims 3 and 14**, Grun further discloses "including sending a write completion signal to the processor for each of the write transactions before the data is flushed to the I/O device **(see fig. 6, which discloses sending a write completion signal to the I/O hub, which communicate t the processor inside the initiator for each of the write transactions before the data is flushed to the I/O device)**, each write completion signal verifying buffering of a corresponding write transaction **(see fig. 6)**.

9. As per **claims 4 and 15**, Grun further discloses "including sending a-flush completion signal to the processor after the data is flushed to the I/O device **(see fig. 6)**.

10. As per **claim 5**, Grun discloses "wherein flushing the data if the flush signal has been received further includes **(see fig. 6)**: tagging the buffer with a first source identifier associated with one or more of the write transactions **(see col. 11, lines 55-67)**; detecting a second source identifier associated with the flushing signal **(see fig. 6, which discloses a which is the second source, the response to the write transaction, as discloses in paragraph 0030 in the applicant's specification)**; comparing the second source identifier to the first source identifier **(as can be seen from fig. 6, comparesing is done by waiting for the second signal to okay transfer from the I/O hub to the target)**; and flushing the data to the I/O device if the second source identifier matches the first source identifier **(see fig. 6 and col. 11, line 61 to col. 12, line 4)**.

11. As per **claim 6**, Grun further discloses "including repeating the comparing for a

plurality of buffers **(col. 12 lines 54-61 discloses repeating the process for each request/command, which uses plurality buffers)**, each buffer corresponding to an I/O port **(fig. 3 shows multiple buffers corresponding to an I/O port)**.

12. As per **claims 7, 16, 28, and 36**, Grun discloses "wherein flushing the data to the I/O device includes: determining whether a latency condition exists **(see col. 12, lines 51-61)**; and flushing the data if the latency condition exists **(see fig. 6 and col. 12, lines 51-61)**, the protocol including a timing protocol **(see col. 12, lines 51-61)** .

13. As per **claims 8 and 17**, Grun further discloses " including sending a write completion signal to the processor for each of the write transactions as the data is flushed to the I/O device **(see fig. 6)**, each write completion signal verifying flushing of a corresponding write transaction **(see fig. 6, which discloses the completion and signal verifying)**.

14. As per **claims 9 and 18**, Grun discloses "wherein the latency condition includes a delay in receiving a next combinable write transaction from the processor and an interface to the I/O device being in an idle state **(see fig. 11)**.

15. As per **claims 10, 20, and 32**, Grun discloses "wherein flushing the data to the I/O device includes flushing more than one cache line worth of data to the I/O device **(with respect to this limitation, page 1, paragraph 0003 from the applicant's specification discloses that a full**

cache line is about 64 byte. Similarly, Grun discloses data to the I/O device includes flushing more than one cache line worth of data to the I/O device. See col. 19, lines 17-32).

16. As per **claims 11 and 33**, Grun discloses "wherein the receiving includes receiving a plurality of commands instructing the I/O hub to consider each write transaction for write combining **(see col. 12, lines 20-33)**, each of the plurality of write transactions including one of the plurality of commands **(see col. 12, lines 30-33)**.

17. As per **claim 12**, Grun discloses "An input/output (I/O) hub **(target channel adapter 22 in fig. 2, which is further explain in fig. 3)** comprising: a buffer **(see fig 3, which discloses buffers inside the target channel adaptor 22)**; and a write combining module **(message and data services (MDS) 30 in fig. 3)** to receive a plurality of write transactions from a processor **(see fig. 2, which discloses write transaction from the processor (initiator) 20 to the I/O hub 22, see also col. 7, lines 1-13)**, store data associated with the write transactions to the buffer and flush the data to an I/O device according to a protocol between the I/O hub and the processor **(see fig. 3, which discloses buffering incoming data inside the I/O hub 22 from the initiator, which also discloses transmitting data from the I/O hub 22 to an I/O controller within the target)**.

18. As per **claim 19**, Grun discloses "The I/O hub of claim 12," **[See rejection to claim 12 above]**, further including a plurality of buffers **(see fig. 3, which shows multiple buffers corresponding to an I/O port)**, each buffer corresponding to an I/O port and the write

combining module is to store data to and flush data from the plurality of buffers according to the protocol between the I/O hub and the processor **(see fig. 3)**.

19. As per **claim 21**, Grun discloses "A system comprising: an input/output (I/O) device **(I/O target 24 in fig. 2, which includes the I/O controller)**; a peripheral components interconnect (PCI) express bus coupled to the I/O device **(see fig. 1)**; a processor **(see fig. 1)**; and a chipset **(the channel-based switched fabric 16 in fig. 2)** having an I/O hub **(target channel adapter 22 in fig. 2, which is further explain in fig. 3)** coupled to the PCI express bus and the processor **(see fig. 2)**, the I/O hub having a buffer and a write combining module **(the target channel adaptor 22)** to receive a plurality of write transactions from the processor **(see fig. 2, which discloses write transaction from the processor (initiator) 20 to the I/O hub 22, see also col. 7, lines 1-13)**, store data associated with the write transactions to the buffer and flush the data to the I/O device according to a protocol between the chipset and the processor **(see fig. 3, which discloses buffering incoming data inside the I/O hub 22 from the initiator, which also discloses transmitting data from the I/O hub 22 to an I/O controller within the target)**, the data to be longer than one cache line **(with respect to this limitation, page 1, paragraph 0003 from the applicant's specification discloses that a full cache line is about 64 byte. Similarly, Grun discloses data to the I/O device includes flushing more than one cache line worth of data to the I/O device. See col. 19, lines 17-32)**.

20. As per **claim 23**, Grun discloses "wherein the processor is to generate the flushing

signal if a flushing event has occurred and a write combine history indicates that one or more combinable write transactions have been issued by the processor **(see fig. 11)**.

21. As per **claims 24 and 25**, Grun discloses "wherein the write combine history is to track combinable write transactions for a particular processor thread and an I/O hub **(see col. 12, lines 20-44)**.

22. As per **claim 26**, Grun discloses "wherein the chipset **(the channel-based switched fabric 16 in fig. 2)** includes a plurality of I/O hubs **(target channel adapter 22 in fig. 2 and host channel adapter 18 in fig. 2, which is further explain in fig. 3)**, the processor to send the flushing signal to each of the plurality of I/O hubs **(see fig. 2 and col. 6, line 60 to col. 7, line 13)**.

23. As per **claim 27**, Grun discloses "wherein the processor is to verify that one or more combinable write transactions have been sent to each of the plurality of I/O hubs before sending the flushing signal **(see fig. 6)**.

24. As per **claim 29**, Grun discloses "wherein the processor is to instruct the I/O hub to consider each write transaction for write combining based on a page table attribute associated with the write transactions **(see col. 13, lines 26-56)**.

25. As per **claim 30**, Grun further discloses "including a point-to-point network

interconnect coupled to the processor and the I/O hub **(see fig. Which discloses point–to-point topology, see also col. 8, lines 13-18)**, the network interconnect having a layered communication protocol **(see col. 7, lines 9-12)**.

26. As per **claim 31**, Grun discloses "A method comprising: receiving a plurality of write transactions from a processor **(see fig. 2, which discloses write transaction from the processor (initiator) 20 to the I/O hub 22, see also col. 7, lines 1-13)**, the plurality of write transactions being destined for an input/output (I/O) device **(see fig. 2)**; storing data associated with the plurality of write transactions to a buffer of the I/O hub **(see fig. 3, which discloses buffering incoming data inside the I/O hub 22 from the initiator, which also discloses transmitting data from the I/O hub 22 to an I/O controller within the target)**; determining whether a latency condition exists **(see fig. 6 and col. 12, lines 51-61)**, the latency condition including-a delay in receiving a next combinable write transaction from the processor and an interface to the I/O device being in an idle state **(see fig. 6)**; flushing the data to the I/O device if the latency condition exists **(see fig. 6)**; and sending a write completion signal to the processor for each of the plurality of write transactions as the data is flushed to the I/O device **(see fig. 6)**, each write completion signal verifying flushing of a corresponding write transaction **(see fig. 6)**.

27. As per **claim 34**, Grun discloses "A machine readable medium to store a set of instructions that direct a computer to function in a specified manner when executed **(see col. 4, lines 36-61)**, the instructions comprising: receiving a plurality of write transactions from a processor **(see fig. 2, which discloses write transaction from the processor (initiator) 20 to**

the target channel adapter 22, see also col. 7, lines 1-13); storing data associated with the write transactions to a buffer of an input/output (I/O) hub **(see fig. 3, which discloses buffering incoming data inside the I/O hub 22 from the initiator, which also discloses transmitting data from the I/O hub 22 to an I/O controller within the target)**; and flushing the data to an I/O device according to a protocol between the I/O hub and the processor **(see fig. 3, which discloses transmitting data from the I/O hub 22 to an I/O controller within the target)**.

IV. RELEVANT ART CITED BY THE EXAMINER

28. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

29. The following reference teaches write transactions on an input/output (I/O) hub according to a protocol between the target and a processor.

U.S. PATENT NUMBER

US 2003/0185154

US 6,683,883

US 6,880,062

US 6,400,730

V. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

30. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

31. Per the instant office action, claims 1-36 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

32. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ernest Unelus whose telephone number is (571) 272-8596. The examiner can normally be reached on Monday to Friday 9:00 AM to 5:00 PM.

IMPORTANT NOTE

33. If attempts to reach the above noted Examiner by telephone is unsuccessful, the Examiner's supervisor, Mr. Fritz M. Fleming, can be reached at the following telephone number: Area Code (571) 272-4145.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions

on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

July 12, 2006

Ernest Unelus
Examiner
Art Unit 2181

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7/23/2006